Hybrid Verification of a Hardware Modular Reduction Engine

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IBM System and Technology Group

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Outline

- Motivation
- Verification Tool
- Verification of Modular Reduction
- Results and Observation

A Brief Introduction to Cryptography

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  - Modular exponentiation $A^B \bmod N$
  - Montgomery multiplier accelerates $A^B \bmod N$ computation.

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- Hardware Accelerator
  - On-chip co-processor that frees up CPU cycles
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  - Long delays: Thousands of clock cycles for a single operation
  - Implemented as a finite-state machine.

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- Bit-level model-checking does not scale to thousands of cycles.
- Very time-consuming to analyze implementation details with a theorem prover.

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- We believe the full potential of hybrid verification tools have not been utilized because:
  - Model checker is not tuned for this kind of proofs.
  - Theorem prover is hard-to-use and time-consuming for many engineers.

ACL2SIX

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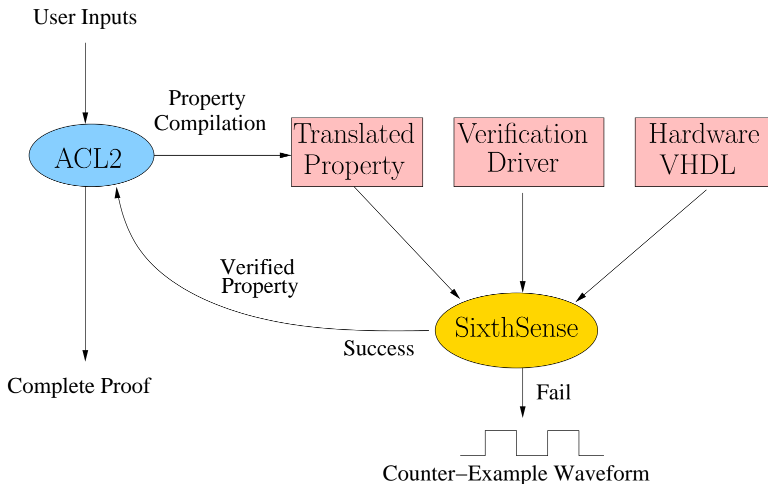
- ACL2SIX directly works on hardware given in HDL.
  - A quick translation of properties, not of hardware HDL.
  - The theorem prover does not deal with low-level details of hardware. The model checker abstracts them away.

ACL2SIX Platform Data Flow



ACL2SIX Theorem Example

Theorem to test the output of a 2-stage 32-bit adder.

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(defthm adder-output
  (implies (natp n)
           (equal (vhdl-sigvec (adder) "SUM" (0 31) (+ n 2))
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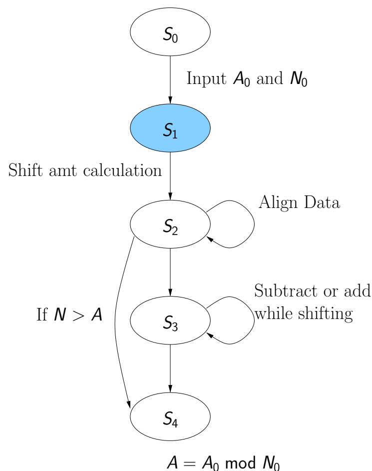
- Directive to call SixthSense from ACL2

Simplified Modular Reduction Engine

Modular reduction engine FSM to compute A_0 mod N_0.

- Example: compute 28 mod 5

$$A = 00011100_2$$
$$N = 00000101_2$$



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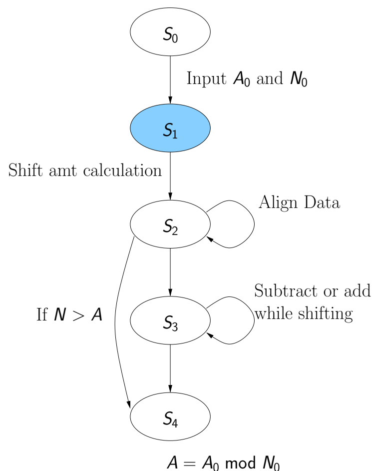

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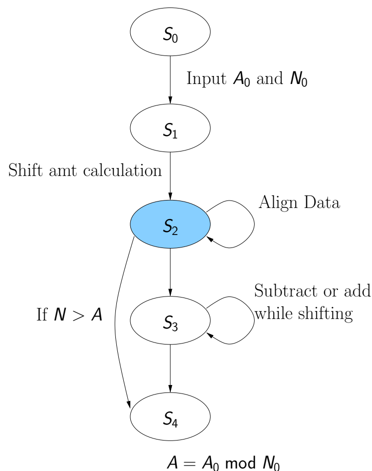

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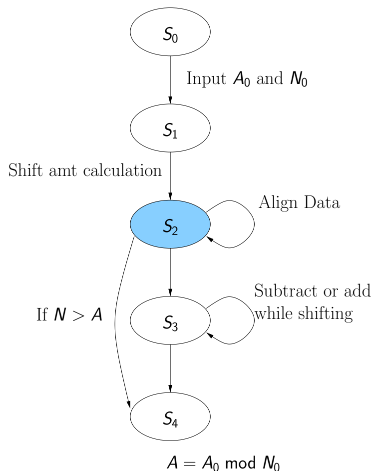

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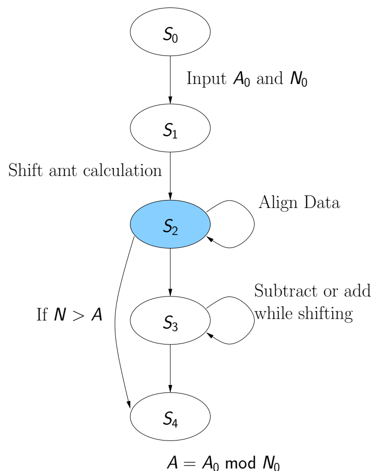

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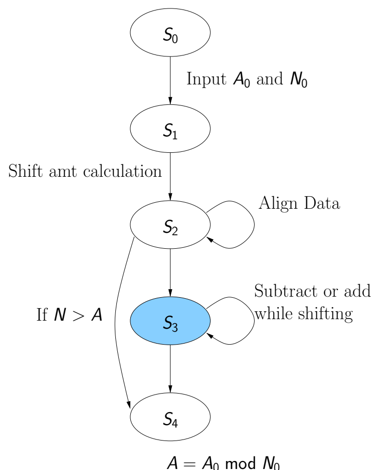

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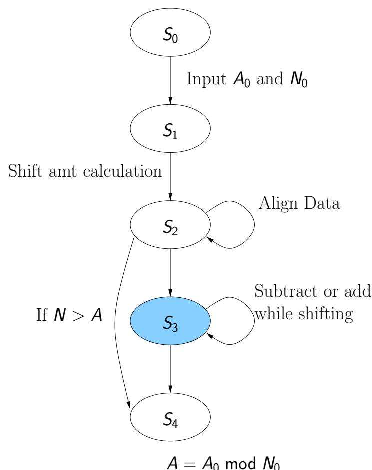

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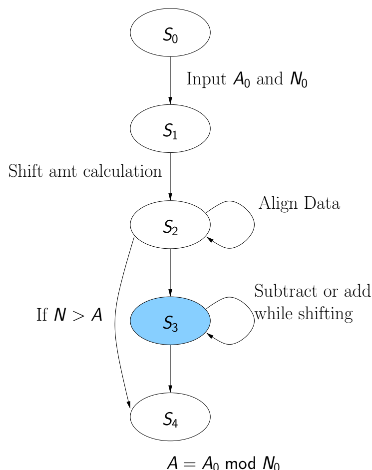

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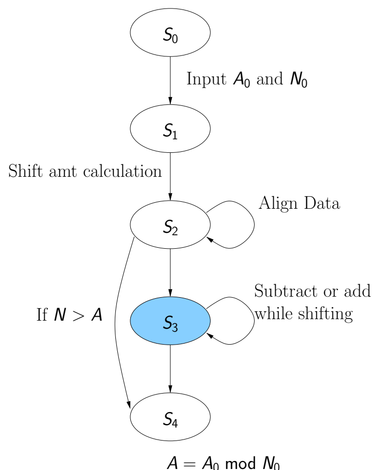

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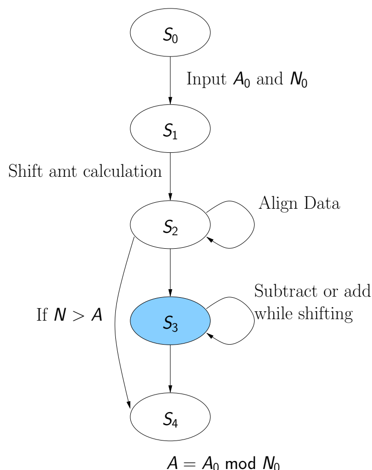

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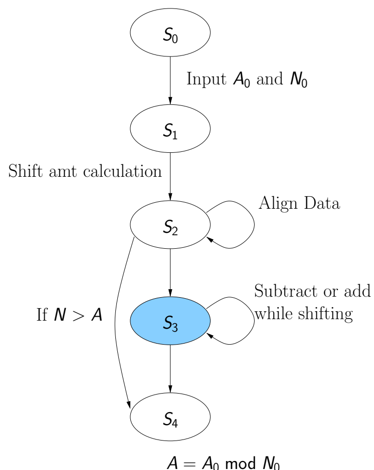

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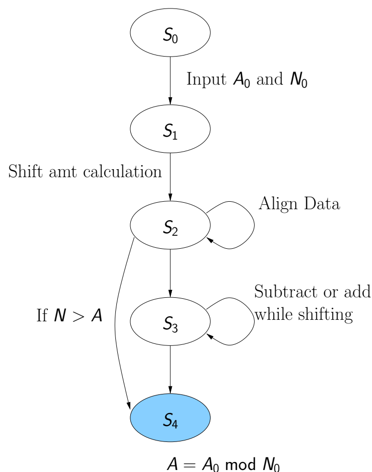

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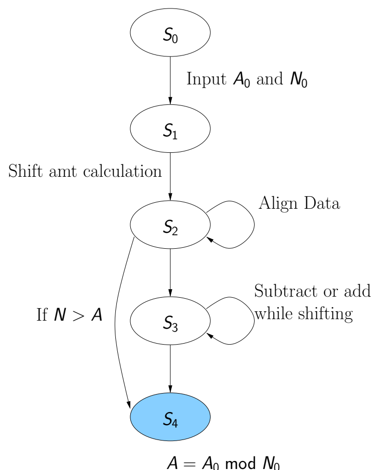

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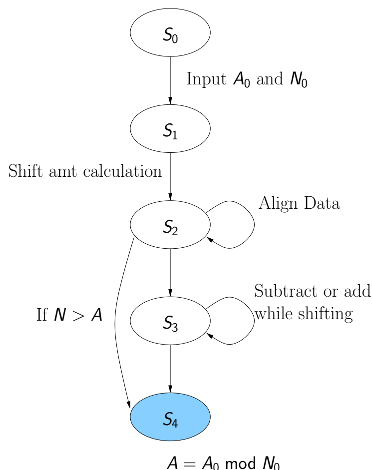

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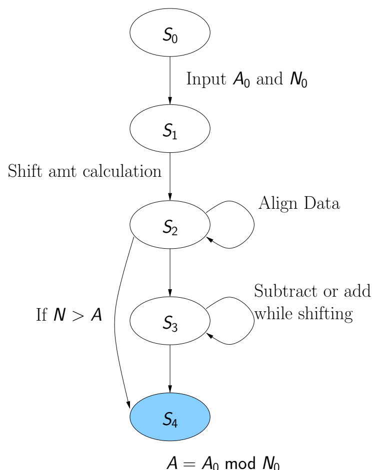
- State transition takes fixed but long clock cycles.



Overall Approach to Verifying a State Transition Machine

- Use a divide-and-conquer approach.
  - Model checker is used to verify properties over each state transition.
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  - Model checker is used to verify properties over each state transition.
  - Theorem prover is used to combine verified properties to form a complete proof, and also reason about high-level math.
- Make the model checker to work on bigger, more abstract sub-problems.
  - Hide the hardware details from the theorem prover.
  - Theorem prover requires smaller steps to create a proof.

How Should We Write Properties over State Transition?

- Typical state transition with pre-condition P_i and post-condition P_{i+1}:

$$P_i(n) \implies P_{i+1}(n + \Delta_i)$$

  - Δ_i is typically constant over 10 but less than 100.

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- Actual conditions are written at high-level.
  - e.g. Multi-word subtraction is simply written as $A - N$ in P_i. The hardware may repeat multiple subtractions over discontinuous data.
- Frequently, we need to add global and state invariants to prove

$$(\mathrm{inv}(n) \wedge \mathrm{cond}_i(n) \wedge P_i(n)) \implies P_{i+1}(n + \Delta_i)$$

  - Invariant definitions are in VHDL and hidden from theorem prover.

Algorithm to verify $P_i(n) \implies P_{i+1}(n+\Delta_i)$

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3. Prove $Q_i'(n)$ by k-induction. Base cases are proved by BMC. Inductive step is proved:
   $Q_i(n) \wedge Q_i(n+1) \wedge \cdots \wedge Q_i(n+k-1) \implies Q_i(n+k)$.

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4. Increase k and repeat Step 3.

Algorithm to verify $P_i(n) \implies P_{i+1}(n+\Delta_i)$

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1. Convert $P_i(n) \implies P_{i+1}(n+\Delta_i)$ to a circuit and combine it with DUT and the driver. Result is $Q_i(n)$.
2. Simplify $Q_i(n)$ by a number of combinational and sequential logic reduction algorithms. Result is $Q'_i(n)$. If $Q'_i(n) = T$, return.
3. Prove $Q'_i(n)$ by k-induction. Base cases are proved by BMC. Inductive step is proved:
$Q_i(n) \wedge Q_i(n+1) \wedge \cdots \wedge Q_i(n+k-1) \implies Q_i(n+k)$.
4. Increase k and repeat Step 3.

Step 1 is performed by the theorem prover. Step 2-4 by the model checker.

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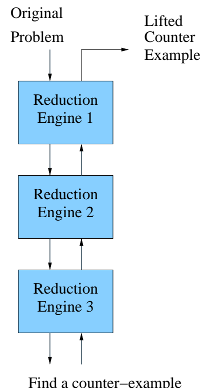
  - Some information is lost during transformation.



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- Often an induction proof fails and a counter-example helps debugging.
- Counter-example generation is difficult for transformation-based verification tool like SixthSense.
    - An inductive counter-example does not start with an initial state.
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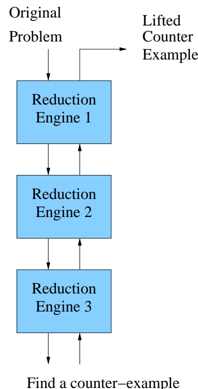
- Implemented a trace lifting to reflect true root cause of induction failure.



Verification Results of Modular Reduction

Data Width	56-bit	256-bit	384-bit	512-bit
Total Time	10442s	20646s	37607s	98199s
Theorem Prover Time	257s	289s	474s	1690s
Property Check Time	10188s	20261s	37139s	97012s
Avg. Time per Prop.	118s	151s	223s	489s
Max Time per Prop.	138s	368s	1232s	3456s

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- Most time spent in the model checker.

Conclusion

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- Still full 4096-bits operation is hard to verify. Need to improve model checker for this type of proof.
- Theorem proving is still a bottleneck to apply in an industrial setting. Need more automation or more productivity.