## Template-based Circuit Understanding

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## Motivation

Verify/reverse-engineer a digital circuit

$$
\Rightarrow
$$

EXTRACT and UNDERSTAND subcomponents

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EXTRACT and UNDERSTAND subcomponents

- FSM extraction [Shi et. al.]
- Functional aggregation and matching [Subramanyan et. al.]
- Word identification and propagation [Li et. al.]
- Identification of repeated structures [Hansen et. al.]


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Most of these techniques do not the find the right permutations in word components

Verify/reverse-engineer a digital circuit

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## EXTRACT and UNDERSTAND subcomponents

What does it mean to understand a combinational circuit $\mathcal{C}$ ?

- Find an equivalent higher-level definition
- Flatten verilog netlist $\rightarrow$ High-level Verilog
- Basic Boolean logic $\rightarrow$

Boolean Logic + Words and operations on Words

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Boolean Logic + Words and operations on Words

Goal
Given purely Boolean Formula $\mathcal{C}$, produce "equivalent" Formula $\mathcal{F}$ over the theory of bitvectors.

A Combinational Boolean circuit $\mathcal{C}(I, O)$ is
(a) a list of input Boolean variables $I=\left\langle x_{1}, \ldots, x_{n}\right\rangle$ and
(b) a list $O=\left\langle f_{1}, \ldots, f_{m}\right\rangle$ of single-output Boolean formulas with inputs $I$.

For $\vec{x} \in\{0,1\}^{n}, \vec{y} \in\{0,1\}^{m}$, by $\mathcal{C}(\vec{x}, \vec{y})$ we denote that $\mathcal{C}$ produces output $\vec{y}$ on input $\vec{x}$

## The library aproach

Check functional equivalence against a library of known components.

- $\mathcal{C}\left(\left\langle x_{1}, \ldots, x_{n}\right\rangle,\left\langle f_{1}, \ldots, f_{m}\right\rangle\right)$
- $\mathcal{C}_{\text {lib }}\left(\left\langle x_{1}, \ldots, x_{n}\right\rangle,\left\langle g_{1}, \ldots, g_{m}\right\rangle\right)$
- Fixed permutations $\sigma, \theta$

$$
\begin{gathered}
\forall i \in\{1, \ldots, m\}, \vec{x} \in\{0,1\}^{m}: \\
f_{\theta(i)}(\sigma(\vec{x}))=g_{i}(\vec{x})
\end{gathered}
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Limitation: Permutations $\sigma, \theta$ must be known.

## Permutation-independent equivalence checking

- $\mathcal{C}\left(\left\langle x_{1}, \ldots, x_{n}\right\rangle,\left\langle f_{1}, \ldots, f_{m}\right\rangle\right)$
- $\mathcal{C}_{\text {lib }}\left(\left\langle x_{1}, \ldots, x_{n}\right\rangle,\left\langle g_{1}, \ldots, g_{m}\right\rangle\right)$
- To be determined permutations $\sigma, \theta$
$\exists \sigma, \theta$ :
$\forall i \in\{1, \ldots, m\}, \vec{x} \in\{0,1\}^{m}:$

$$
f_{\theta(i)}(\sigma(\vec{x}))=g_{i}(\vec{x})
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\end{aligned}
$$



Limitation: Still too restrictive.

1. $\mathcal{C}$ usually does not have a "standard" functionality.
2. $\mathcal{C}$ 's functionality must be fully matched.

## Template-based synthesis

Instead of a reference circuit, our approach requires a template of a specific form.


## How do our templates look like?

A template $T$ of a combinational circuit $\mathcal{C}(I, O)$ is:

- A subset $O_{T} \subseteq O$,
- a partition $I=\left(I_{C} \cup \bigcup_{i=1}^{n}\left(W_{i}\right)\right)$, and
- a conjuntion of guarded assignments of the form

$$
a_{i}: \psi_{i}\left(I_{C}\right) \Rightarrow\left(\theta\left(O_{T}\right):=\phi_{i}\left(\sigma\left(W_{i_{1}}\right), \tau\left(W_{i_{2}}\right)\right)\right)
$$

where

- $\psi_{i}$ is a to be determined assignment on $I_{C}$,
- $\theta, \sigma, \tau$ are to be determined permutations, and
- $\phi_{i}$ is a binary function over words.
- $i_{1}, i_{2} \in\{1, \ldots, n\}$.

1. Circuit $\mathcal{C}(I, O)$
2. Subset outputs $:=O$
3. Partition $I:=$ control $\cup$ inputs $A \cup$ inputs $B$
4. Template with
(a) To be determined assignments v1, v2
(b) To be determined permutations $\mathrm{p}, \mathrm{q}$

| ```(and (=> (value v1 control) (= outputs (bv-add (permute p inputsA) (permute q inputsB) ) 1 ) (=> (value v2 control) (= outputs (ite (bv-slt (permute p inputsA) (permute q inputsB) ) (mk-bv 32 1) (mk-bv 32 0) ) ) , )``` |
| :---: |
|  |  |
|  |  |

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$$
\exists p, q, v 1, v 2:
$$

$$
\forall \vec{x} \in\{0,1\}^{n}, \vec{y} \in\{0,1\}^{m}:
$$

$$
\mathcal{C}(\vec{x}, \vec{y}) \Rightarrow T(p, q, v 1, v 2, \vec{x}, \vec{y})
$$



Check validity of Boolean formulas over the theory of bit-vectors with two levels of quantification ( $\exists \forall$ QF_BV):

$$
\exists \vec{x}: C(\vec{x}) \wedge \forall \vec{y}: A(\vec{x}, \vec{y})
$$

1. High-level preprocessing and simplifications [Wintersteiger et. al.]
2. Counterexample-refinement loop, similar to the approach used in 2QBF solvers [Ranjan et. al., Janota et. al.]
3. Functional signatures [Mohnke et. al.]
(1) Miniscoping:

$$
\begin{aligned}
& \exists \vec{x}: A \vee B \rightarrow \exists \vec{x}: A \vee \exists \vec{x}: B \\
& \forall \vec{x}: A \wedge B \rightarrow \forall \vec{x}: A \wedge \forall \vec{x}: B
\end{aligned}
$$

(2) Equality resolution:

$$
\begin{aligned}
& \exists \vec{x}: C(\vec{x}) \wedge \forall \vec{y}:\left(\bigwedge_{i}\left(y_{i}=x_{i}\right) \Rightarrow B(\vec{y})\right) \\
& \rightarrow \\
& \exists \vec{x}: E(\vec{x}) \wedge \forall \vec{y}: \bigcup_{i}\left(\left\{y_{i} \rightarrow x_{i}\right\}\right)(B(\vec{y}))
\end{aligned}
$$

(3) Distinguishing signatures.

## Distinguishing Signatures

An output signature $s_{\text {out }}$ is a function $s_{\text {out }}: \mathcal{B}_{n} \rightarrow \mathcal{D}$ such that, for every function $f$ and permutation $\tau$ :

$$
\left.s_{\text {out }}\left(f\left(x_{1}, \ldots, x_{n}\right)\right)=s_{\text {out }}\left(f\left(\tau\left(x_{1}\right), \ldots, \tau\left(x_{n}\right)\right)\right)\right)
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\exists x, y: s_{\text {out }}\left(f_{x}\right) \neq s_{\text {out }}\left(g_{y}\right) \Rightarrow \theta(y) \neq x
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& \exists x, y: s_{\text {out }}\left(f_{x}\right) \neq s_{\text {out }}\left(g_{y}\right) \Rightarrow \theta(y) \neq x
\end{aligned}
$$

- We consider one input signature and one output signature.
- Input dependency
- Output dependency
- Signatures can be computed independently in the circuit and the template.


Benchmarks (40 Sat/40 Unsat):

## Experiments

- Reverse engineering benchmarks generated from high-level (behavioral) Verilog using the Synopsys Compiler.
- From ISCAS, an academic processor implementation, and synthetic examples.
- ALUs, multipliers, shifters, counters...

Tools:

- Yices
- Z3
- Bloqqer + DepQBF
- Bloqqer + RareQs
- Bloqqer + sKizzo
- Cir-CEGAR (Mini-SAT)
(Yices format)
(SMT2 format)
(QDimacs)
(QDimacs)
(QDimacs)
(QDimacs + top titeral)

Variants:

- Considered two simple encodings for permutations
- Studied effect of preprocessing, encodings, and signatures


## Conclusion and further work

- Yices and Z3 are sensitive to the encoding of permutations
- Preprocessing and signatures are harmless and crucial in many cases
- Benchmarks are available in SMT2, YICES, QBF and (soon) QCIR
- Just putting together two SAT/SMT solvers is not enough
- QDIMACS encoding is not suitable for this kind of synthesis
- Integrate signature computation in the Exist-Forall loop
- Compare to other synthesis algorithms


## Questions? Comments? Suggestions?





